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A Viable Mission Profile Emulator for Power Modules in Modular Multilevel Converters

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***Abstract*—Various methods have been presented in the past to emulate the electrical behavior of Modular Multilevel Converters (MMCs). To meet the demands for the reliability aspect study of MMCs, this paper proposes a minimum viable setup to emulate the thermal behavior and to investigate its feasibility for reliability testing and thermal model validation of the power modules in the MMC. The proposed mission profile emulator has three distinctive features: 1) Capable of emulating and measuring the thermal stresses of power modules; 2) Capable of implementing practical switching profile as a full-scale MMC; and 3) Having significantly reduced requirement for DC power supply compared to existing setups used for electrical studies. Theoretical discussions, and simulations as well as the experimental results are presented to demonstrate the capability of the mission profile emulator both electrically and thermally. Moreover, this paper is accompanied by a video demonstrating how to measure the junction temperature of the power devices using the optical fiber and the thermal camera.**

***Index Terms*—Mission profile, modular multilevel converters, power semiconductor devices, reliability.**

I. Introduction

SINCE Modular Multilevel Converters (MMCs) have distinguish advantages, such as scalability, modularity, low switching frequency, excellent output harmonic performance, etc., it has today become a key equipment of High Voltage Direct Current (HVDC) transmission [1] [2]. The reliability of MMC is important for the HVDC transmission and further for the grid security of a region and even a country. However, the massive use of IGBT power modules introduces challenges to the reliability of the MMC since they are one of the vulnerable components in power electronic systems according to an industry survey [3]. Electro-thermal stress is one of the major mechanisms resulting in fatigue and failure [4]. Therefore, it is of great necessity to conduct reliability validation of the MMC before its field operation, especially from the electro-thermal testing point of view.

The reliability aspect testing based on a full-scale MMC [5] is usually not economically possible since huge manpower, financial resources, and plenty of time are needed to accomplish the complicated system. Therefore, a minimum viable Sub-Module (SM)-based setup that can emulate the key electro-thermal stresses of the IGBT modules applied in MMCs is an interesting solution in order to avoid the high cost of time and capital [6]. The essence of the SM-based testing is to use a two-level circuit to emulate a multilevel circuit. The challenge lies in how to retain the key reliability features of one SM in the full-scale MMC, such as the arm current, the switching frequency and the capacitor voltage (blocking voltage of the IGBTs). In a typical MMC system, the power devices rated at 4.5 kV/1.2 kA are most commonly used in the SM [7] [8], which requires a high-voltage power supply to drive the reliability testing. Moreover, MMCs can achieve nearly 1 % THD with only several hundred hertz of switching frequency [9]. It means that the two-level SM-based test bench has to improve the switching frequency in order to achieve a similar harmonic quality. These issues severely limit the application scope of the SM-based test bench and may fail some crucial electro-thermal requirements in the full-scale MMC, which are summarized as below: 1) High-voltage and high-current, 2) Low switching frequency (e.g., several times of the fundamental frequency [10]), 3) Smooth arm current, and 4) DC bias in the arm current. In the prior-art studies, several SM-based test solutions focusing on the electrical behavior have been proposed. In [6], a dual SM-based resonant circuit is proposed to reduce the requirement of the inductor filter. However, owing to inherent characteristics of the resonant circuit, it is impossible to inject a DC bias current into the SM, which consequently cannot emulate the practical operation condition of the MMC. In order to implement the DC component, a half-bridge converter is utilized as the current source [11], where

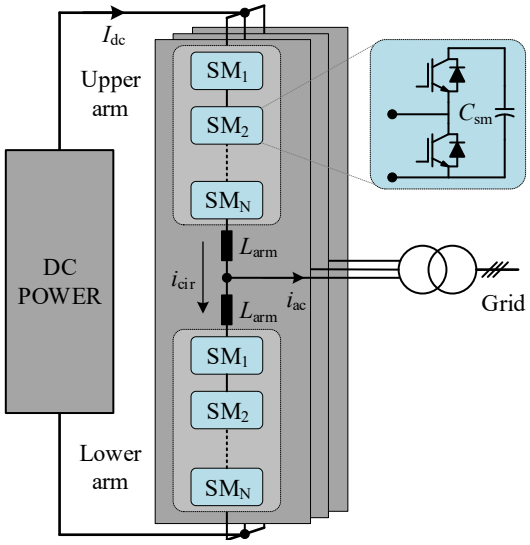

Fig. 1. Circuit configuration of a typical three-phase MMC. $I_{\rm dc}$ is the DC-bus current, $i_{\rm ac}$ is the output AC current, $i_{\rm cir}$ is the circulating current, $L_{\rm arm}$ is the arm inductor, and $C_{\rm sm}$ is the submodule capacitor.

its system parameters (e.g., power supply voltage, coupling inductor and SM capacitor) are easy to be scaled according to a practical MMC system. Nonetheless, it is not able to cope with the low switching frequency mission profiles, where plenty of undesirable harmonics may be introduced into the arm current. Several reliability test setups focusing on the reliability aspect behavior are also proposed. Tang et al. [12] utilizes a full bridge converter to emulate the arm current profile. In this case, the problems related to the DC bias current and the low switching frequency are addressed only if the power supply voltage is higher than the SM voltage. However, it should be noted that this voltage requirement significantly restrains the application scope of this test setup, especially for high-voltage power semiconductors. As an improvement, a reverse-connected auxiliary SM is utilized [13]. By proper control, the DC voltages of the Device Under Test (DUT) and auxiliary SM are canceled out by each other and do not exist in the output voltage. Thus, the power supply voltage can be lower, and the test capability is greatly improved more than five times in terms of the applicable voltage level of the DUT. However, the power supply voltage is still coupled with the DUT, and should be carefully chosen.

In this paper, a novel SM-based mission profile emulator is proposed. It is capable of emulating and measuring the thermal stresses of power modules, and it is capable of implementing practical switching profile as a full-scale MMC. Moreover, the requirement for DC power supply is significantly reduced compared to the existing viable setups. The rest of this paper is organized as follows: the proposed topology and its control scheme are presented in Section II; Section III provides the practical consideration for the mission profile emulator implementation, and the impact of the introduced current ripple and the omitted capacitor voltage ripple on the power losses are analyzed as well. Section IV demonstrates the mission profile emulator through a series of experiments electronically and thermally. Finally other capabilities that the setup has are shown in Section V followed by the conclusion in Section VI.

II. Topology and Control Scheme of the Proposed Mission Profile Emulator

In order to build an SM-based mission profile emulator of the MMC, the voltage and the current conditions as well as the switching behavior of the SM in a full-scale MMC has to be identified first and then fully emulated. Thus, this Section will first present the basic operation of a full-scale MMC, and then accordingly the proposed mission profile emulator.

A. Basic Configuration and Operation of a Full-Scale MMC

The typical configuration of a three-phase MMC is shown in Fig. 1. Each phase is divided into two arms: the upper arm and the lower arm. Each arm consists of N series-connected half-bridge SMs and an arm inductor to limit the circulating current and the fault current. In order to transfer the active power, instead of the AC component, a DC circulating current exists in the arm current. Taking the upper arm of phase *A* for example, the arm current is

$$\begin{aligned} i_{\mathrm{arm}} &= \frac{I_{\mathrm{dc}}}{3} + \frac{I_{\mathrm{ac}}}{2}\sin\left(\omega t + \varphi_1\right) + I_2 \sin\left(2\omega t + \varphi_2\right) \\ &= I_0 + I_1 \sin\left(\omega t + \varphi_1\right) + I_2 \sin\left(2\omega t + \varphi_2\right), \end{aligned} \tag{1}$$

where i_{arm} is the arm current, I_{dc} is the DC-bus current, I_{ac} is the amplitude of the output AC current, I_2 is the amplitude of the second order harmonic current, I_0 and I_1 refer to the DC component and the fundamental component of the arm current, ω is the angular frequency, φ_1 and φ_2 are the initial phase angle of the fundamental component and the second-order component in the arm current respectively. Other higher order harmonics are omitted in this paper.

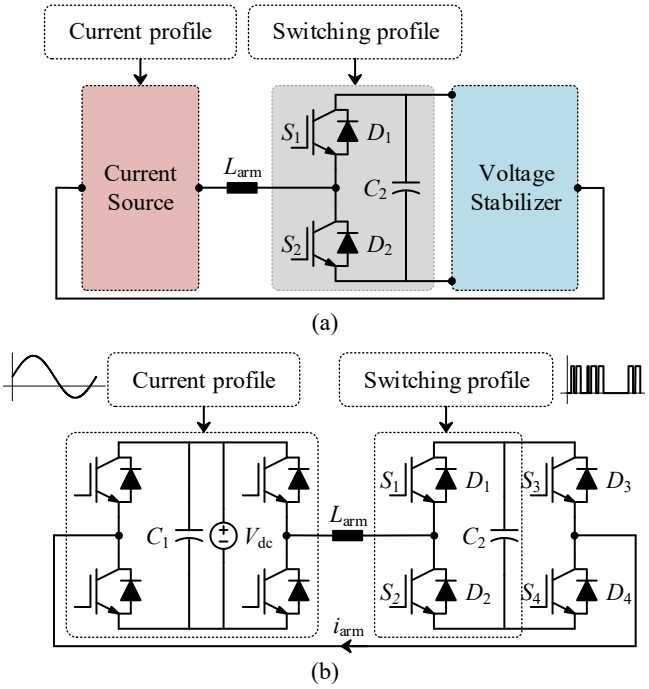

Fig. 2. Configuration of the proposed mission profile emulator. (a) Simplified circuit diagram and (b) Detailed circuit diagram.

B. Proposed Mission Profile Emulator

The proposed mission profile emulator is composed of a "controlled current source", a coupling inductor, the SM under test, and a voltage stabilizer as shown in Fig. 2(a). The controlled current source is achieved by a full-bridge converter regulated by a PI controller, and functions to track the current profile. The DUT (four power devices in one SM) is strictly controlled by the switching profile. The capacitor C_2 here works differently from the one in a practical SM. It serves only to maintain the blocking voltage of the DUT at the average value of an actual SM in order to obtain similar switching losses as in practice. Thus, in the actual test, the capacitor C_2 will first be charged to the required blocking voltage during the start-up process, and be controlled to keep constant afterwards until the end of the test. In order to regulate the capacitor voltage V_{C2}, the voltage stabilizer consisting of two auxiliary IGBTs are paralleled with the DUT to provide

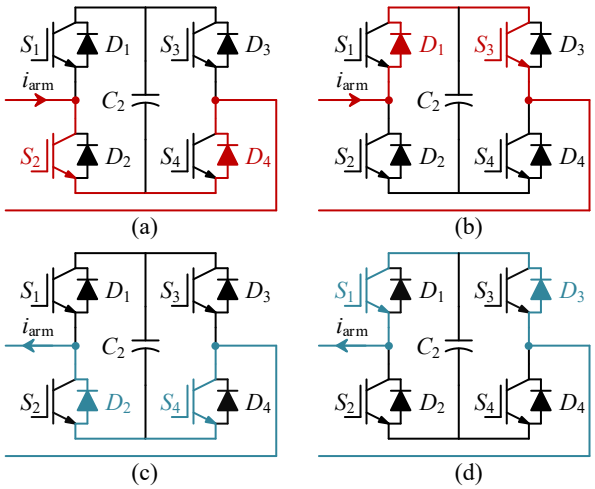

Fig. 3. Ideal current paths in the DUT and the voltage stabilizer. (a) Bypass state of SM with a positive current; (b) Insert state of SM with a positive current; (c) Bypass state of SM with a negative current; (d) Insert state of SM with a negative current.

extra current paths. In theory, S_3 can share the same gate signal with S_1 from the switching profile, which is complementary to S_2 and S_4. Through such an arrangement, this topology can make sure that a current path without going through the capacitor C_2 always exists as shown in Fig. 3 taking the positive current for example. It means that the capacitor C_2 will not be charged/discharged regardless of the switching profile and the current profile, and its voltage V_{C2} will remain the same all the time. Eventually, two main advantages can be achieved by this topology. One is that the switching profile is decoupled with the current profile, and any practical switching profile can be tested on this mission profile emulator. Another one is that the voltage of power supply V_{dc} is decoupled with the voltage of the DUT since the capacitor C_2 is not inserted into the current path in theory. Thus, V_{dc} can be as low as possible theoretically only if the inductor is properly selected accordingly, which will be discussed later in this section. This can greatly facilitate the test of a SM rated at high voltage level. According to the above information, a comparison between the proposed mission profile emulator and other test methods are summarized in Table I.

Nevertheless, in practice, turn-on delays have to be arranged for all gate signals to avoid short circuit between two devices in the same half bridge. In this case, non-ideal current paths will appear, and the current will be forced to charge the capacitor C_2 during the delay interval as shown in Fig. 4(a). Consequently, the capacitor voltage will increase and deviate from its rated value quickly, especially when a high frequency switching profile is applied. Thus, a capacitor voltage controller is needed for the mission profile emulator.

C. Capacitor Voltage Control

According to the analysis above, the voltage of capacitor C_2 increases during the test. One of its impacts is the different switching loss from its practical operation due to the growing blocking voltage. Moreover, the increasing voltage may diverge and trigger the system protection mechanism,

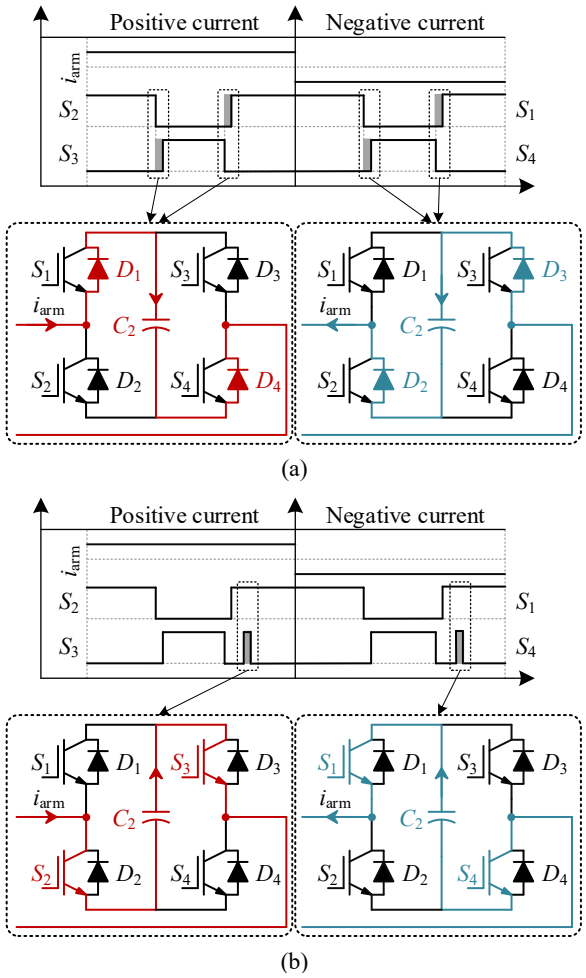

Fig. 4. Operation of the mission profile emulator. (a) Current paths to charge the capacitor C_2 during the interval of turn-on delay; (b) Current paths to discharge the capacitor C_2 during the additional high-level switching actions.

and finally break down the electro-thermal test. Therefore, a capacitor voltage control should be embedded into the overall control strategy.

The gate signal S_1 and S_2 are decided by the switching profile allowing no interference from external controller. The voltage stabilizer will, therefore, serve to achieve this control objective. The principle is to introduce extra switching actions (high-level or low-level switching actions) to S_3 and S_4 in addition to the original switching profile. In this case, the current will be forced to charge or discharge the capacitor C_2. Fig. 4(b) shows the current paths to discharge the capacitor C_2 regarding different current directions. Specifically, when the current is positive, an extra high-level switching status is added to S_3, and the current path is changed from Fig. 3(a) to Fig. 4(b) to discharge the capacitor. When the current is negative, the additional high-level switching status in S_4 will alter the current path from Fig. 3(b) to Fig. 4(b) to discharge the capacitor. In contrast, extra low-level switching statuses in S_3 and S_4 regardless of the current direction will charge the capacitor C_2.

For high switching frequency mission profiles like Phase Shifted Carrier (PSC) modulation [14], this capacitor voltage

TABLE I
COMPARISON BETWEEN PROPOSED MISSION PROFILE EMULATOR AND OTHER TEST BENCHES WHEN SM VOLTAGE IS 2 KV.

Testing capabilities		Proposed	[13]	[12]	[11]	[6]
DC power supply voltage requirement		Wide range	545 V	$>$ 2 kV	= 2 kV	—
Applicable switching profile	High switching frequency	√	√	√	√	√
	Low switching frequency	√	√	√	×	×
Applicable current profile	DC current	√	√	√	√	×
	Second-order current	√	√	√	√	×

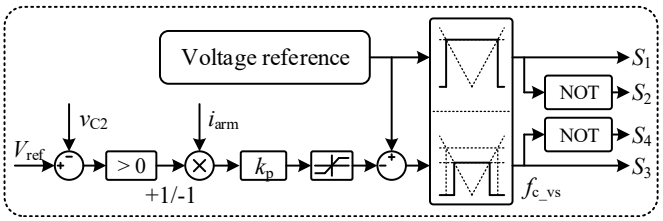

Fig. 5. Capacitor voltage control designed for high switching frequency mission profiles.

control can be achieved by inserting turn-on/turn-off delays and leads into the gate signal since plenty of switching edges can be used. However, it is not effective enough to the mission profiles with a low switching frequency, such as the Nearest Level Modulation (NLM) [15]. A longer period of time will be taken to regulate the capacitor voltage. Thus, in the following part, two modulation strategies are designed for mission profiles with a high switching frequency and a low switching frequency respectively.

1) High Switching Frequency Mission Profile: For the MMC, high switching frequency applications, such as the PSC modulation, are normally carrier-based, and controlled by the arm voltage reference. Thus, the voltage control can be achieved by subtracting an adjustment to the voltage reference, then compare it with the carrier in order to get the final gate signal for S_3 and S_4 as shown in Fig. 5. The adjustment is dynamically decided by the capacitor voltage error, the arm current and the switching profile. In detail, a positive adjustment contributes to an extra turn-on delay and turn-off lead of S_3 to charge the capacitor, and a negative adjustment can add additional turn-on leads and turn-off delays to S_3 to discharge the capacitor. The advantage of this method lies in the same switching frequency between the DUT and the two auxiliary IGBTs in the voltage stabilizer. Thus, the similar power loss among the devices can be expected.

2) Low Switching Frequency Mission Profile: The efficiency of the capacitor voltage control depends on the duration and the equivalent switching frequency of the additional switching actions. However, since the arm current ripple is affected by the high-voltage capacitor C_2 during the voltage regulation, the duration of additional switching actions cannot be as long as possible. Moreover, the switching frequency is relatively low when it comes to the low switching frequency applications (e.g., several times of the fundamental frequency [16]). Thus, the method shown in Fig. 5 is not effective and efficient any more. One alternative way is to combine the original switching profile with additional high frequency switching actions in order to obtain the final S_3 and S_4. As shown in Fig. 6, the modified switching series (the red switching series for charging the capacitor and the blue switching series for discharging the capacitor) are allocated to the two auxiliary devices when the capacitor voltage goes out of the upper and lower voltage limitations, and the capacitor voltage control is disabled when the C_2 voltage is within its limitations. Note that the additional switching action will be ineffective when it is the same with the switching profile.

D. Control Parameter Selection

Besides the PI control parameters, one main control parameter that needs to be designed is the proportional gain k_p in the capacitor voltage control as shown in Fig. 5 and Fig. 6. It should be well tuned to ensure the current ripple introduced by the capacitor voltage control within a certain range since it determines the duration T_a of additional switching action. Within the short time interval, the voltage of C_2 is assumed to remain constant, and the resulting current variation ΔI is

$$\Delta I = \frac{V_{\mathrm{C2}}}{L_{\mathrm{arm}}} T_\mathrm{a} = k_\mathrm{a} \left| i_{\mathrm{arm}} \right|, \tag{2}$$

where V_{C2} is the constant voltage of the capacitor C_2, L_{arm} is the inductance, and k_a is the current ripple ratio, which restricts the peak value of the current error introduced by the capacitor voltage control (e.g., $k_\mathrm{a} = 0.05$ means that a maximum 5% error of the arm current will be introduced).

The duty ratio introduced by T_a is equal to $k_\mathrm{p} \left| i_{\mathrm{arm}} \right|$

$$T_\mathrm{a} f_{\mathrm{c\_vs}} = \frac{k_\mathrm{a} \left| i_{\mathrm{arm}} \right| L_{\mathrm{arm}} f_{\mathrm{c\_vs}}}{V_{\mathrm{C2}}} = k_\mathrm{p} \left| i_{\mathrm{arm}} \right|, \tag{3}$$

where $f_{\mathrm{c\_vs}}$ is the carrier frequency used for the capacitor voltage control in the voltage stabilizer and k_p is the proportional gain to achieve a limited current ripple

$$k_\mathrm{p} = \frac{k_\mathrm{a} L_{\mathrm{arm}} f_{\mathrm{c\_vs}}}{V_{\mathrm{C2}}}. \tag{4}$$

By using (4), the current error caused by the capacitor voltage control can be limited within $k_\mathrm{a} \times 100\%$ of the actual current.

E. Hardware Parameter Selection

Besides the control parameters, the selection of hardware parameters matters in order to fulfill the test requirements.

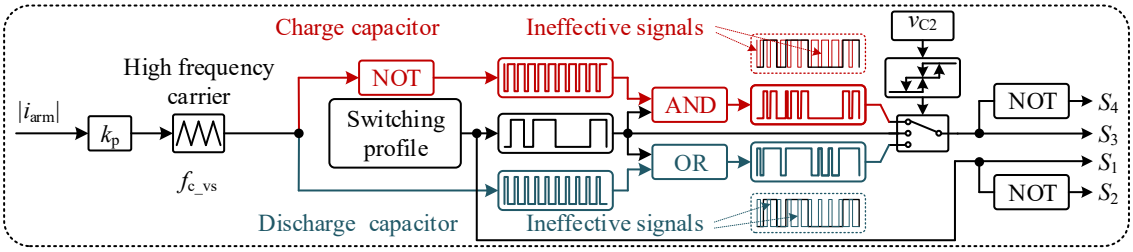

Fig. 6. Capacitor voltage control designed for low switching frequency mission profiles.

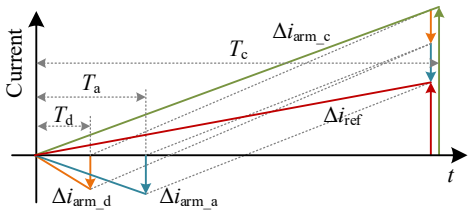

Fig. 7. Current changes caused by the DC power supply, the current reference, the turn-on delay, and the capacitor voltage control in one carrier period.

There are four main kinds of component in this setup, namely the IGBT, the capacitor, the inductor and the power supply. Their parameters should be chosen according to the ratings of the DUT and the mission profiles to be studied.

First of all, the IGBT modules used in the current source and the voltage stabilizer are supposed to have high enough voltage and current ratings based on the testing requirement. In this case, for one, it is, therefore, possible to cover a series of potential SMs under test with various IGBT modules (such as with different voltage and current ratings, with different packages, from different manufacturers and the like). For the other, the current source and voltage stabilizer with higher rating IGBTs tends to have longer lifetime expectation even when the same cooling system with the DUT is employed. In practice, the cooling system of the current source and the voltage stabilizer should be designed independent of the DUT, in order to avoid its thermal coupling impact on the DUT as well as to keep a low mean junction temperature of its IGBTs even when being fully loaded and regulated with the highest allowed carrier frequency. In this case, the test bench might be able to be recycled for multiple testings due to its limited thermal stress of the IGBT modules and correspondingly longer lifetime.

Moreover, due to the far lower blocking voltage than the IGBTs in the DUT and its higher ratings, the carrier frequency used in the current source can be much higher than that of the DUT in order to ensure an excellent current profile tracking performance. In a word, through this design, the carrier frequency and the thermal stress of the two parts will not restrain the application scope of the mission profile emulator any more.

The inductor and the power supply interact with each other, and their parameter limitations come from two aspects. For one, the maximum inductance $L_{\mathrm{arm\_max}}$ is determined by the system dynamic tracking capability. It mainly refers to the current tracking performance. In the worst case, the current change caused by the power supply must be equal to the sum of the current change caused by the current reference, the turn-on delay and the capacitor voltage control as shown in Fig. 7. The current variations caused by different reasons in one carrier period are

$$\begin{cases} \Delta i_{\mathrm{arm\_c}} = \dfrac{V_{\mathrm{dc}}}{L_{\mathrm{arm}}} T_{\mathrm{c\_vs}} \\ \Delta i_{\mathrm{ref}} = \dfrac{di_{\mathrm{arm}}}{dt} T_{\mathrm{c\_vs}} \\ \Delta i_{\mathrm{arm\_a}} = k_{\mathrm{a}} i_{\mathrm{arm}} \\ \Delta i_{\mathrm{arm\_d}} = \dfrac{V_{\mathrm{C2}}}{L_{\mathrm{arm}}} T_{\mathrm{d}} \\ \Delta i_{\mathrm{arm\_c}} \geq \Delta i_{\mathrm{ref}} + \Delta i_{\mathrm{arm\_a}} + \Delta i_{\mathrm{arm\_d}}, \end{cases} \tag{5}$$

where $\Delta i_{\mathrm{arm\_c}}$, Δi_{ref}, $\Delta i_{\mathrm{arm\_a}}$, and $\Delta i_{\mathrm{arm\_d}}$ are the current changes caused by the power supply, current reference, capacitor voltage control and the turn-on delay; V_{dc} is the voltage of the power supply; $T_{\mathrm{c\_vs}}$ is the carrier period of the current source; T_{d} is the duration of the turn-on delay.

Substituting (1) into (5), the maximum allowed inductance can be estimated by

$$L_{\mathrm{arm\_max}} = \frac{V_{\mathrm{dc}} T_{\mathrm{c\_vs}} - V_{\mathrm{C2}} T_{\mathrm{d}}}{\left(k_{\mathrm{a}} I_0 + \sqrt{\omega^2 T_{\mathrm{c\_vs}}^2 + k_{\mathrm{a}}^2} I_1 + \sqrt{4\omega^2 T_{\mathrm{c\_vs}}^2 + k_{\mathrm{a}}^2} I_2\right)}. \tag{6}$$

The minimum inductance $L_{\mathrm{arm\_min}}$ is decided by the requirement of the arm current ripple resulting from the Pulse Width Modulation (PWM). Assuming a well-behaved current controller, the practical current increment is equal to the increase of current reference. Thus, minimum inductance is

$$L_{\mathrm{arm\_min}} = \frac{T_{\mathrm{c\_vs}} V_{dc}}{4 I_{\mathrm{r\_max}}}, \tag{7}$$

where $I_{\mathrm{r\_max}}$ is the amplitude of the current ripple caused by the PWM.

In addition, by allowing the reactive power flow in this mission profile emulator, the power supply in this topology only works to provide the power loss of the whole system and to maintain the steady state voltage of the parallel capacitor. In the meantime, the instantaneous positive and negative power for the inductor current control is provided by the parallel capacitor. It means that the power rating of the power supply can be greatly reduced, which can be only several percentage of the power rating of the SM under test.

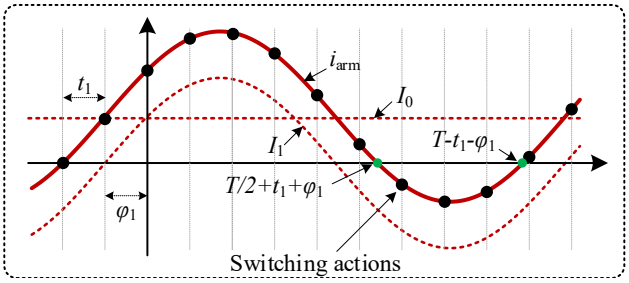

Fig. 8. Ideal arm current waveform with DC circulating current and simplified evenly-distributed switching actions.

F. Voltage Stabilizer Carrier Frequency Selection

Due to the low equivalent switching frequency of the MMCs with NLM, a specific capacitor voltage control for it is proposed in Section II-C in order to regulate the capacitor voltage more efficiently. However, how to distinguish the two kinds of mission profiles and how to choose the carrier frequency for the voltage stabilizer are not clear yet. Thus, in this part, explanations will be given in detail based on the time that the control takes to regulate the capacitor voltage. As a matter of fact, two factors, namely the turn-on delay and the additional switching actions, can change the voltage of the capacitor C_2. Turn-on delays always charge the capacitor and the additional switching actions can either charge or discharge the capacitor.

First of all, the voltage change caused by one turn-on delay can be calculated by

$$\Delta v_{\mathrm{C2\_d\_i}} = \frac{1}{C_2}\int_{t}^{t+T_{\mathrm{d}}} |i_{\mathrm{arm}}|dt \approx \frac{T_{\mathrm{d}}}{C_2}\left|I_{\mathrm{arm\_i}}\right|, \tag{8}$$

where $\Delta v_{\mathrm{C2\_d\_i}}$ is the voltage increase caused by the i^{th} turn-on delay in one fundamental period; C_2 is the capacitance; T_{d} is the period of turn-on delay; $I_{\mathrm{arm\_i}}$ is the amplitude of the current when the turn-on delay occurs. Since the period of delay is very short, normally around several micro seconds, the current during this period is assumed to be constant. In addition, the turn-on delay charges the capacitor all the time regardless of the current direction, thus the absolute value of the current is used in the equation to take the impact of the negative current into account.

Similarly, the voltage change caused by one additional switching action from the capacitor voltage control can be estimated by

$$\Delta v_{\mathrm{C2\_a\_i}} = \frac{1}{C_2}\int_{t}^{t+T_{\mathrm{a\_i}}} |i_{\mathrm{arm}}|dt \approx \frac{k_{\mathrm{a}}L_{\mathrm{arm}}}{C_2V_{\mathrm{C2}}}|I_{\mathrm{arm\_i}}|^2, \tag{9}$$

where $\Delta v_{\mathrm{C2\_a\_i}}$ is the voltage change caused by the i^{th} additional switching action in the time interval of $T_{\mathrm{a\_i}}$.

The capacitor voltage increase/decrease in one fundamental period can be estimated by summing up all caused changes as

$$\begin{aligned}\Delta V_{\mathrm{C2\_in/de}} &= \sum_{i=0}^{N_{\mathrm{a}}} \Delta v_{\mathrm{C2\_a\_i}} \pm \sum_{i=0}^{N_{\mathrm{DUT}}} \Delta v_{\mathrm{C2\_d\_i}} \\ &\approx \frac{f_{\mathrm{c\_vs}}}{f_1}\frac{k_{\mathrm{a}}L_{\mathrm{arm}}}{C_2V_{\mathrm{C2}}}\overline{|i_{\mathrm{arm}}|^2} \pm \frac{f_{\mathrm{e\_DUT}}}{f_1}\frac{T_{\mathrm{d}}}{C_2}\overline{|i_{\mathrm{arm}}|},\end{aligned} \tag{10}$$

where $\Delta V_{\mathrm{C2\_in/de}}$ is the voltage increase (corresponding to the plus) or the voltage decrease (corresponding to the minus) in one fundamental period; N_{a} is the number of the additional switching actions in one fundamental period, which is equal to $f_{\mathrm{c\_vs}}/f_1$; N_{DUT} is the number of the switching actions of the DUT in one fundamental period, which is equal to $f_{\mathrm{e\_DUT}}/f_1$ determined by the mission profile; f_1 is the fundamental frequency being 50 Hz in this paper; $f_{\mathrm{c\_vs}}$ is the carrier frequency of the voltage stabilizer; $f_{\mathrm{e\_DUT}}$ is the equivalent switching frequency of the DUT; $\overline{|i_{\mathrm{arm}}|^2}$ and $\overline{|i_{\mathrm{arm}}|}^2$ are the average of $|i_{\mathrm{arm}}|^2$ and $|i_{\mathrm{arm}}|$ in one fundamental period.

The time that the control takes to change the capacitor voltage by a certain value ΔV_{C2} can be estimated by

$$T_{\mathrm{in/de}} = \frac{\Delta V_{\mathrm{C2}}}{f_1\Delta V_{\mathrm{C2\_in/de}}}, \tag{11}$$

where $T_{\mathrm{in/de}}$ is the time consumed for a certain capacitor voltage increase/decrease and is inversely proportional to the carrier frequency of the voltage stabilizer. Apparently, discharging the capacitor will take a longer time than charging it due to the negative impact of the turn-on delay.

Finally, the minimum carrier frequency of the voltage stabilizer can be derived when a specific requirement of the minimum $T_{\mathrm{in/de}}$ is set by the operators or testers to ensure an reasonable performance of the capacitor voltage control. This minimum carrier frequency is the threshold to distinguish the two kinds of mission profiles. An example of the carrier frequency selection for the experimental setup used in this paper will be given in Section IV-A.

TABLE II
MAIN PARAMETERS OF IGBTS USED IN THE FULL-SCALE MMC AND THE PROPOSED MISSION PROFILE EMULATOR.

MMC system	Full-scale	Mission profile emulator
Power module	5SNA_1200G450350	F4_50R12KS4
$V_{\mathrm{on\_0}}$	1.5 V	1.9 V
R_{on}	0.52 mΩ	31.6 mΩ

III. Practical Considerations in the Mission Profile Emulator Implementation

A. Impact of Current Ripple on the Conduction losses

Compared with the excellent current harmonic performance in the practical MMC, the current ripple caused by the PWM exists in the proposed test setup. Thus, its impact on the conduction loss should be investigated. Moreover, the impact of the omitted capacitor voltage ripple on the switching loss should also be evaluated since a constant blocking voltage is used in the proposed mission profile emulator. Scenarios of a

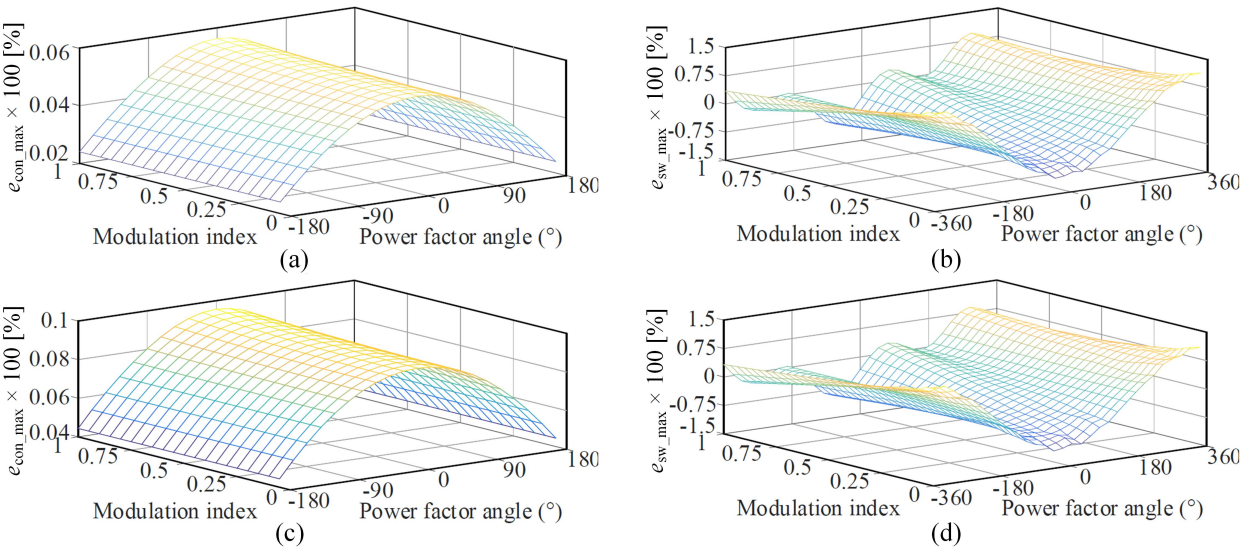

Fig. 9. Maximum conduction loss error introduced by the current ripple regarding different modulation indexes and power factor angles: (a) and (b) Full-scale MMC, and (c) and (d) Mission profile emulator.

full-scale MMC system and the proposed test bench will be both analyzed.

For IGBT, the conduction loss is only related to the on-state characteristics and the current regardless of the blocking voltage. Thus, the conduction loss error introduced by the arm current ripple is only analyzed instead of the voltage ripple of the capacitor C_2. The on-state characteristics of IGBT and diode are linearized and modeled by $V_{\rm on} = V_{\rm on\_0} + R_{\rm on}\,|i_{\rm arm}|$, where $V_{\rm on}$ is the on-state voltage drop of the semiconductor; $V_{\rm on\_0}$ is the on-state zero-current voltage drop in the linearized model, and $R_{\rm on}$ is the equivalent on-state resistance.

The total conduction loss dissipation $P_{\rm con\_sm}$ of the four semiconductors in one fundamental period is

$$P_{\rm con\_sm} = \frac{1}{T}\int_{-t_1-\varphi_1}^{T-t_1-\varphi_1} V_{\rm on}\,|i_{\rm arm}|dt, \tag{12}$$

where T is the fundamental period; t_1 is the interval between the time when the arm currents with/without DC component are both equal to zero as shown in Fig. 8. The triangle current ripple is over-estimated as a sinusoidal waveform with the same frequency and amplitude. Thus, $P_{\rm con\_sm}$ can be simplified as

$$P_{\rm con\_sm} = P(I_0, I_1) + P(I_{\rm r\_max}), \tag{13}$$

where $P(I_0, I_1)$ is the conduction loss which is unrelated to the current ripple, and $P(I_{\rm r\_max})$ is the conduction loss introduced by the current ripple. Some detailed expressions are shown in Appendix.

The maximum conduction loss error introduced by the ripple current is

$$\frac{P(I_{\rm r\_max})}{P(I_0, I_1)} \le \frac{P_{\rm max}(I_{\rm r\_max})}{P(I_0, I_1)} = e_{\rm con\_max}, \tag{14}$$

where $P(I_{\rm r\_max})$ and $e_{\rm con\_max}$ are the maximum conduction loss and the maximum conduction loss error introduced by the current ripple.

IGBT modules in the full-scale MMC system and the proposed test bench are used to evaluate the conduction loss error. The main parameters are listed in Table II, and the results are shown in Figs. 9(a) and 9(c), where $I_{\rm r\_max}$ is set at 20% of the peak value of arm current. It can be seen that the maximum error is always below 0.1% for both scenarios regardless of the modulation index and the power factor angle. Thus, it is reasonable to ignore the impact of the introduced current ripple on the thermal behavior of the DUT, and it is acceptable to limit the amplitude of the current ripple within 20% of the peak value of the current.

B. Impact of Capacitor Voltage Ripple on the Switching losses

As for the capacitor voltage, it operates in order to get a similar switching loss behavior as in real operation. It is determined by the current, blocking voltage and the junction temperature as [17]

$$\begin{aligned} &E_{\rm sw}(i_{\rm arm}, v_{\rm sm}, T_{\rm j}) = \\ &E_{\rm sw}(i_{\rm arm}, V_{\rm ref}, T_{\rm ref})[1 + K_{\rm T}(T_{\rm j} - T_{\rm ref})]\frac{v_{\rm sm}}{V_{\rm ref}}, \end{aligned} \tag{15}$$

in which $E_{\rm sw}(i_{\rm arm}, V_{\rm ref}, T_{\rm ref})$ is the switching energy obtained by curve-fitting of the data-sheet of IGBT module (e.g., 5SNA 1200G450350 from ABB [18] and F4_50R12KS4 from Infineon [19]) under certain blocking voltage $V_{\rm ref}$ and junction temperature $T_{\rm ref}$, $v_{\rm sm}$ is the actual SM voltage, $K_{\rm T}$ is a temperature coefficient, and $T_{\rm j}$ is the junction temperature.

An evenly distributed switching action is assumed throughout the fundamental period in order to exclude the complex calculation of the exact switching time [20]. All three kinds of energy losses ($E_{\rm sw\_on}$, $E_{\rm sw\_off}$ and $E_{\rm sw\_rec}$) occur simultaneously with the total energy loss of $\sum E_{\rm sw\_x}(i_{\rm arm}, v_{\rm sm}, T_{\rm j})$ per switching action. Considering a constant junction temperature

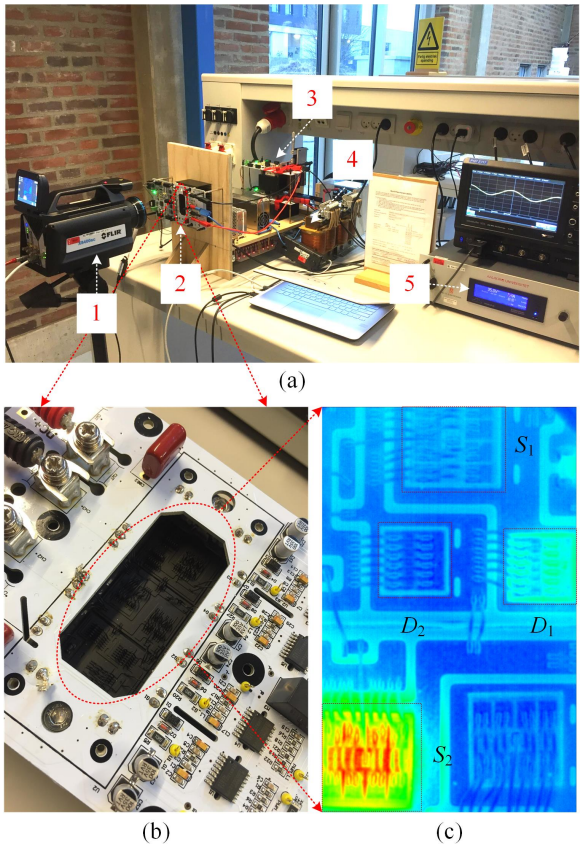

Fig. 10. Experimental setup of the proposed mission profile emulator: (a) photo of the setup, (b) photo of the SM, and (c) thermal distribution of the DUT under operation. (1: Thermal Camera, 2: Device Under Test, 3: Current source and the voltage stabilizer, 4: Inductor, and 5: Power Supply.)

in steady state, the switching energy error caused by omitting the voltage ripple in one fundamental period is

$$e_{\mathrm{sw}} = \frac{\sum_{1}^{N_{\mathrm{s}}} \sum E_{\mathrm{sw\_x}}(i_{\mathrm{arm}}, v_{\mathrm{sm}}, T_{\mathrm{j}}) v_{\mathrm{sm\_ripple}}}{\sum_{1}^{N_{\mathrm{s}}} \sum E_{\mathrm{sw\_x}}(i_{\mathrm{arm}}, v_{\mathrm{sm}}, T_{\mathrm{j}}) v_{\mathrm{sm}}}, \tag{16}$$

where N_{s} is the number of switching transients in one fundamental period.

Figs. 9(b) and 9(d) show the maximum switching loss error caused by omitting 10% voltage ripple across the SM capacitor. It can be seen that the maximum error is always within 1.5% regardless of the modulation index and the power factor used. Thus, the mission profile emulator with a constant capacitor voltage is suitable for the electro-thermal validation of the MMC.

IV. Mission Profile Emulator Demonstration

In order to validate the effectiveness of the proposed test bench, an experimental setup is build as shown in Fig. 10(a). Three IGBT modules (F4_50R12KS4 from Infineon) are used. One module serves as the "controlled current source" with the carrier frequency being 6 kHz (it can be adjustable). Another module is used as the DUT operating at half-bridge status, which aims to exclude the impact of thermal coupling from the voltage stabilizer implemented by the third module. For safe operation, a 2 us turn-on delay is embedded into all gate signals. Due to the hardware limitation, the blocking voltage of the power devices is set to 300 V.

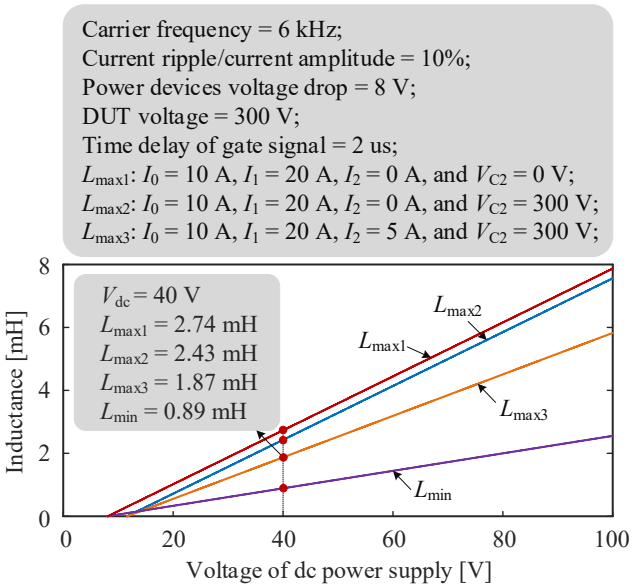

Fig. 11. Relationship between the inductance and the DC power supply voltage under different testing conditions.

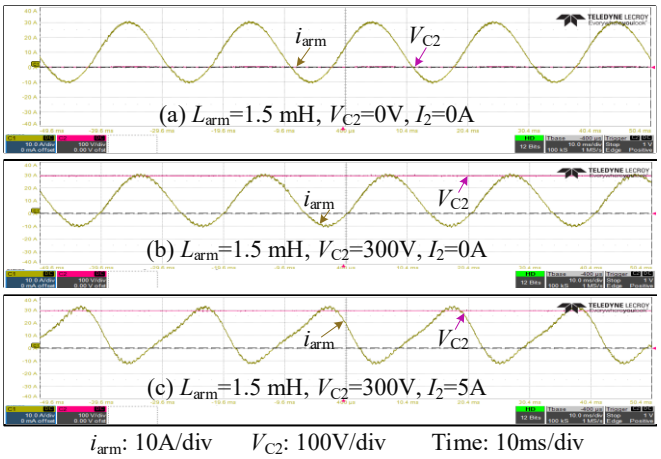

Fig. 12. Experimental waveforms of the current and the capacitor voltage under different operating conditions.

A. Parameter Selection Example

In order to get the exact thermal behavior of the DUT as in practice, the total current ripple caused by the PWM and the capacitor voltage control is limited to be within $\pm 10\%$. Here 5% comes from the capacitor voltage control, and another 5 % margin is allocated to the inherent current error introduced by the modulation. Based on the information above and (6)-(7), the relationship between the inductance and the power supply voltage is derived and shown in Fig. 11. In this paper, the of 40 V far lower voltage than the capacitor voltage 300 V is used in the current source. In this case, the minimum inductance fulfilling the current requirement is 0.89

TABLE III
MAIN SYSTEM PARAMETERS OF THE MISSION PROFILE EMULATOR IN THE EXPERIMENT.

Item	Value	Item	Value
DC power supply voltage V_{dc}	40.0 V	Carrier frequency of current source $f_{\mathrm{c\_cs}}$	6.0 kHz
Capacitor voltage V_{C2}	300.0 V	Carrier frequency of voltage stabilizer $f_{\mathrm{c\_vs}}$	1.5/2.0 kHz
Inductor L_{arm}	1.5 mH	Equivalent frequency of DUT $f_{\mathrm{e\_DUT}}$	1.5/0.1 kHz
Capacitor C_2	1.4 mF	Fundamental frequency f_1	50 Hz
DC current amplitude I_0	10.0 A	Turn-on delay T_{d}	2.0 us
Fundamental current amplitude I_1	20.0 A	Ambient temperature T_{amb}	20 °C
Current ripple radio k_{a}	0.05	IGBT module	F4_50R12KS4

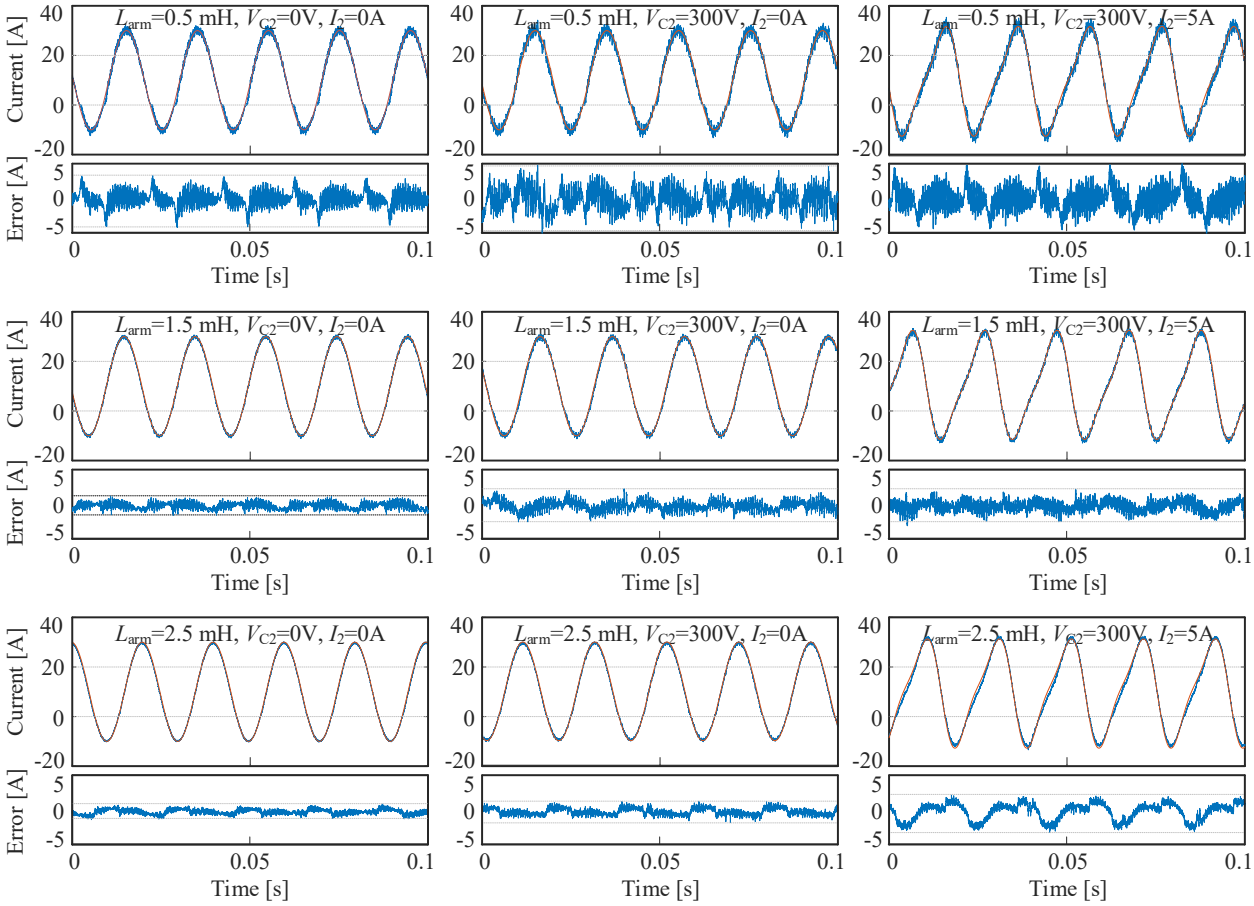

Fig. 13. Experimental waveforms of the actual current, its current reference and the current error under various operating conditions.

mH and the maximum inductances are 2.74 mH, 2.43 mH, and 1.87 mH respectively for three different current profiles. Accordingly, discrete inductances are chosen to validate the hardware selection method, namely 0.5 mH, 1.0 mH, 1.5 mH, 2.0 mH, 2.5 mH, and 3.0 mH. 1.5 mH is chosen as the final inductance used in the experimental emulator. Note that the voltage drop across the power devices (8 V in total for two diodes and two IGBTs in the current path.) should be taken into account when calculating the maximum inductance in case of a low power supply voltage (e.g., 40 V in this paper).

Together with other main system parameters shown in Table III, the carrier frequency used for the capacitor voltage control can be determined. In the experiment, the voltage control should be able to effectively charge and discharge the capacitor by 5 V increase/decrease within 0.1 s or 5 fundamental cycles (which is adjustable) to stabilize its voltage at 300 V. According to (8)-(11), the minimum carrier frequency of the voltage stabilizer calculated is 1.5 kHz for the high switching frequency mission profile applications. When it comes to the low switching frequency mission profile, considering the existence of ineffective additional switching actions (such as for NLM) as mentioned in Section II-C, longer time will be taken to charge or discharge the capacitor in this case. Thus, the carrier frequency is increased to 2.0 kHz.

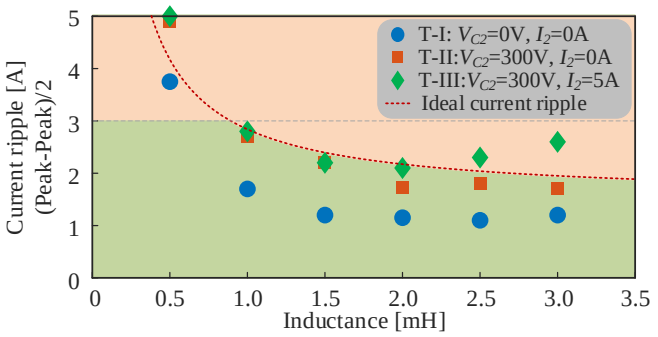

Fig. 14. Measured current error between the actual current and its reference under different test conditions. (Ideal current error is the error introduced by the capacitor voltage control and the PWM.)

B. Current Tracking Performance

Fig. 12 shows the waveforms of the current and the capacitor voltage under different conditions when the inductance is 1.5 mH. It can be seen that the current and the voltage are well regulated with/without the second-order harmonic circulating current injection. Moreover, the current tracking errors caused by the PWM and the capacitor voltage control can be obtained by comparing the testing results from Figs. 12(b) and (c) with Fig. 12(a). To illustrate the current tracking error in detail, part of the experimental results in terms of using discrete inductances are exported from the oscilloscope, and compared with its references as shown in Fig. 13. The current tracking errors are summarized in Fig. 14. The ideal current ripple refers to the sum of the ripple caused by PWM for different inductances (calculated by (7)), and the ripple from capacitor voltage control (5 % of the current peak, namely 1.5 A in this paper). It can be seen that when the inductance is 0.5 mH, which is smaller than the minimum inductance 0.89 mH according to Fig. 11, the current ripple will be larger than the allowed value (10 % of the current peak, namely 3 A) for all three testing conditions. In addition, if 5 A second-order circulating current is injected, and the voltage V_{C2} is 300 V, the inductance should be smaller than 1.87 mH to fulfill the current ripple requirement as shown Fig. 14.

C. Capacitor Voltage Control Performance

Fig. 15 shows the experimental start-up process of the capacitor voltage control used in the high switching frequency applications with the DUT operating with PSC. It can be observed that the capacitor voltage is controlled to increase gradually from 0 V to 300 V in the start-up process. It consumes about 2.5 seconds in total in order to reach the steady state, which is pretty close to 2.7 seconds predicted by (8)-(11). From the zoom-in Fig. 15(b), the modulation principle shown in Fig. 5 can be clearly seen, where the turn-on delays and turn-off leads are embedded into S_3 to charge the capacitor compared with S_1.

Similar experiments are conducted under the same operation conditions but with the nearest level modulation as shown in Fig. 16. The waveforms of the capacitor voltage and the arm current are similar with those tested with PSC. Due to the increased carrier frequency being 2.0 kHz, the start-up process

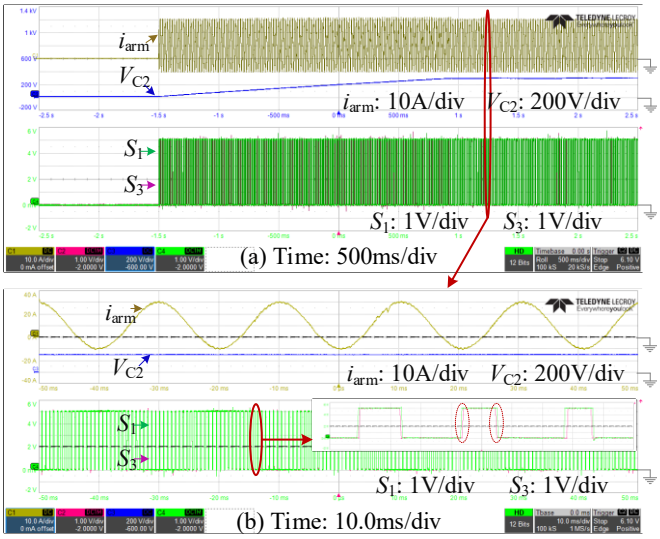

Fig. 15. Experimental waveforms of the arm current, the capacitor voltage and the gate signals with DUT operating with phase shifted carrier modulation.

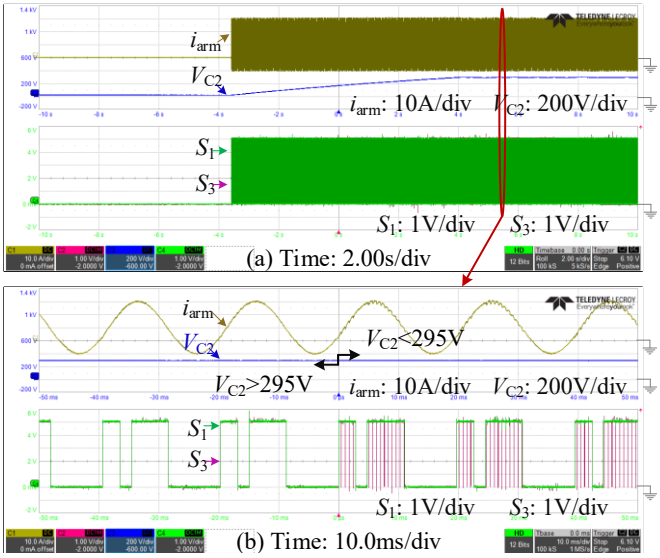

Fig. 16. Experimental waveforms of the arm current, the capacitor voltage and the gate signals with DUT operating with nearest level modulation.

still takes longer time around 7.5 seconds. This is caused by two reasons. For one, many ineffective signals exists as shown in Fig. 6, where the inserted extra switching actions are the same as the original mission profile. For the other, less turn-on delays are deployed due to the low switching frequency mission profile. Note that the duration of the start-up process has very little impact on the thermal stress of the power devices in terms of a long-term testing. It can also be seen from the zoom-in Fig. 16(b) that when the capacitor voltage stabilizes around 300 V, the capacitor voltage control is disabled automatically until the voltage is lower than 295 V or exceeds 305 V (5 V voltage band). The modulation principle can be clearly seen from the gate signals. To be more specific, plenty of high frequency low-level switching pulses are inserted into S_3. On the contrary, S_3 keeps the same as S_1 when the capacitor voltage control is disabled.

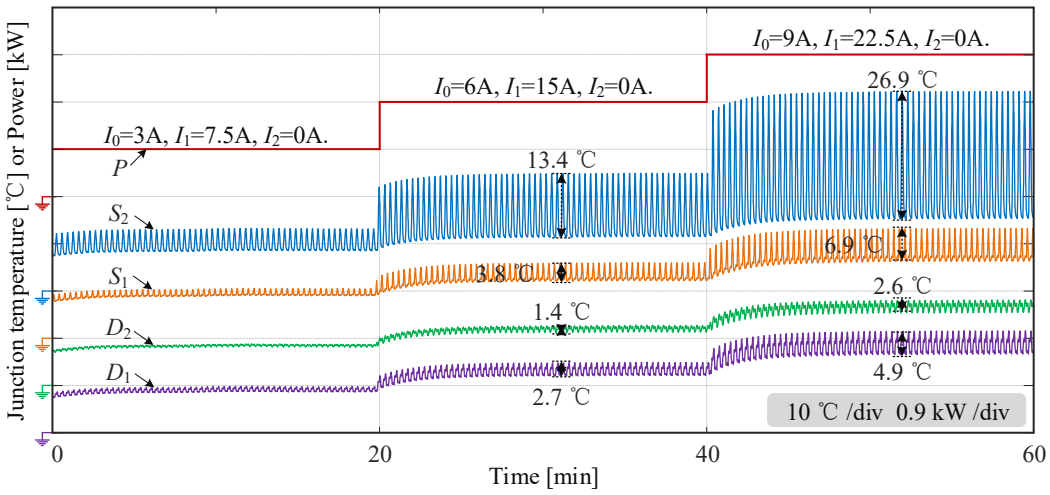

Fig. 17. Measured junction temperatures of four DUTs under different power levels in 60 minutes with the cycle period being 20 s.

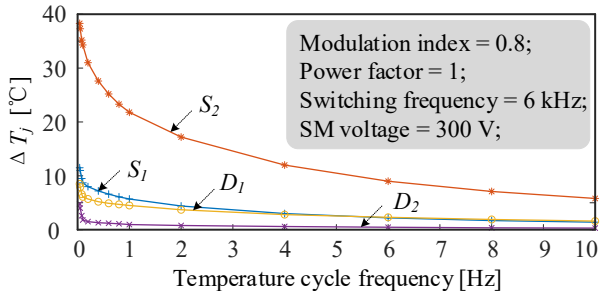

Fig. 18. Junction temperature variation of the four power devices tested under different temperature cycle frequencies.

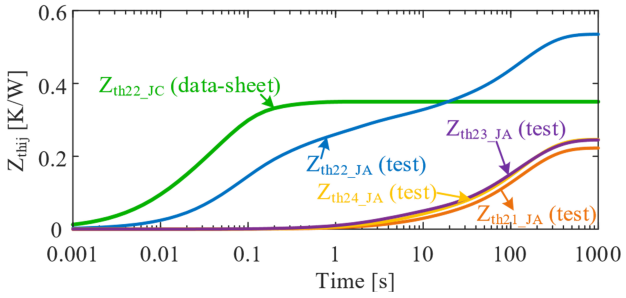

Fig. 19. Self and mutual thermal impedances related to device S_2. (Z_{22_JC} is the junction-to-case thermal impedance obtained from the data-sheet, and Z_{22_JA} is the junction-to-ambient thermal impedance from the experiment.)

V. Mission Profile Emulator Capabilities

The proposed test bench is aimed at assessing the reliability of the power semiconductors in the MMC under various operating conditions. As one of the most significant factors contributing to the reliability issues, the thermal stress is the main focus of the reliability assessment, and this test setup is able to facilitate relevant thermal researches such as the accelerated AC power cycling testing, and the electro-thermal model validation, the SM cooling system design and the like. In the following, two application scenarios are detailed.

A. Capability I — AC Power Cycling Testing

Power cycling testing is a powerful approach to assess the failure mode of the power device in a short period of time. By analyzing the testing results, a lifetime model in respect to the temperature can be built for the remaining lifetime prediction under certain mission profiles. In general, DC power cycling testing is the most commonly used due to its simplicity, and plenty of test circuits can be used in this case [21]. However, the disadvantage of this method is clear that the DUT does not operate under the realistic electrical conditions [22], and uncertainties will be added to the test result analysis. Thus, AC power cycling test, which enables the power devices operating under more actual load conditions attracts more attention nowadays [23]. The proposed mission profile emulator is able to conduct the AC power cycling testing for the power devices with an acceptable power consumption for a long testing.

In the practical power cycling applications, several main testing indicators should be adjustable according to different testing requirements, namely the mean junction temperature, the cycle period, and the junction temperature swing. The mean junction temperature can be controlled by changing the heat-sink temperature through an external heating and cooling system. The cycle period can be regulated in two ways as mentioned in [22]. For one, the temperature cycle period is the same as the current frequency, which can be adjusted easily. For another, by applying high frequency current for a certain period of time, different temperature cycles can be achieved. As for the junction temperature swing, it can be controlled by changing the amplitude, switching frequency, power factor and modulation index of the current. In addition, the junction temperature can be tested either by an optical fiber or an infrared thermal camera as shown in the attached video. In this paper, the junction temperature is tested through an infrared thermal camera from FLIR, and the temperature distribution inside the IGBT module is shown in Fig. 10(c).

Fig. 17 shows the experimental temperature response of the four DUTs under various power levels, namely 0.9 kW, 1.8 kW, and 2.7 kW in 60 minutes. The measured currents are shown in Fig. 17 with the modulation index and the

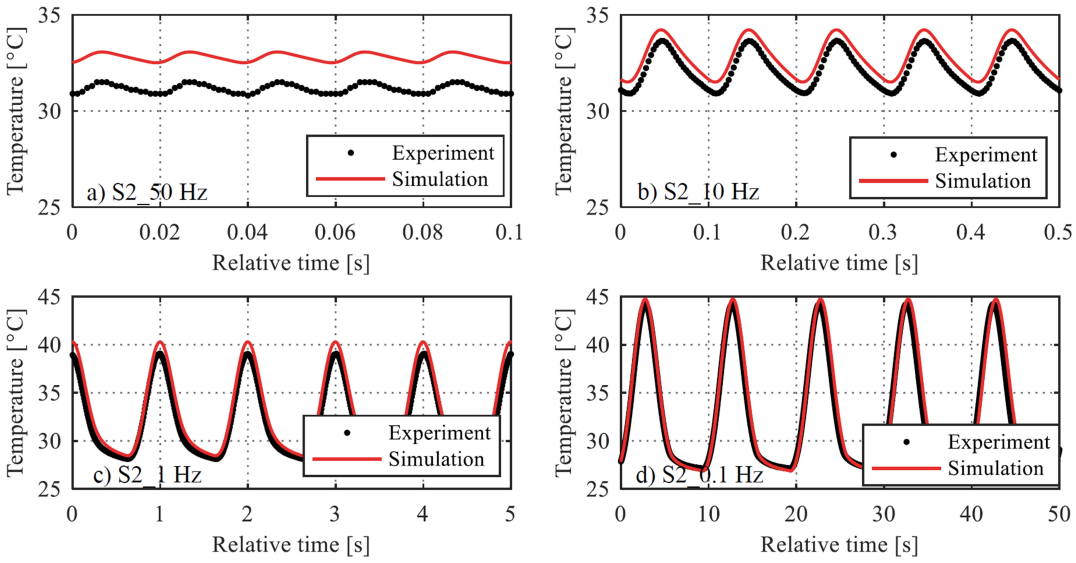

Fig. 20. Experimental and simulated waveforms of the steady state junction temperature of the device S_2 under different current frequencies. (a) 50 Hz, (b) 10 Hz, (c) 1 Hz, and (d) 0.1 Hz.

power factor being 0.8 and 1.0 respectively. Other system parameters are listed in Table III. The cycle period is 20 s with the temperature frequency being 0.05 Hz. The temperature reference is the ambient temperature of 20 °C. It can be seen that by changing the power level, different junction temperature swings can be achieved, such as 4.6 °C, 13.4 °C, and 26.9 °C for the three power levels. The mean junction temperature alters as well. In order to accelerate the power cycling testing, higher temperature swings can be achieved by increase the current amplitude, switching frequency as well as the blocking voltage.

To briefly illustrate the impact of the cycle period on the temperature swing, Fig. 18 shows the achievable junction temperature swing amplitude under different temperature cycle frequencies of this setup. The testing conditions are $I_0 = 11.4$ A, and $I_1 = 28.6$ A. It can be seen that the lower the frequency is, the higher the junction temperature swing can be achieved. In addition, due to the evenly distributed thermal stress among the four power devices, device S_2 will be the first one reaching the end of life.

B. Capability II — Electro-Thermal Model Validation

The thermal model derived from the cooling curve test can be used for the junction temperature estimation and other thermal managements. However, under normal circumstances, the thermal model provided by the manufacturer cannot be used to predict the temperature accurately due to the difference of the cooling systems between the practical applications (the air-forced heat-sink cooling in this paper) and the one used by the manufacturer (the water cooled copper heat-sink) [24]. Negative impact of excellent water cooling on the thermal spread among the module contributes to a lower case temperature, which results in a higher thermal impedance than the actual case [25]. Another point is that, unlike the Cauer model, the Foster model provided by the manufacturer only describes the transfer function between the input power and the output temperature, but no information about the output power. Thus, different Foster models (e.g. independent thermal models of junction-to-case and the heat-sink) cannot be connected in series directly, and a complete thermal model taking the specific cooling system into account has to be done through a thermal path from the junction to the ambient via the thermal grease and the heat sink. Last but not least, thermal coupling has to be taken into consideration for a multi-chip module, in which different junction temperatures interact through the baseplate and the heat-sink. However, the thermal model from the manufacturer is only tested under self-heating condition. Due to the three reasons mentioned above, thermal model of IGBT modules has to be characterized before utilization and validated for practical applications.

Linear superposition is a widely used tool to describe the thermal behavior of a multi-source system dominated by thermal conduction [26], [27]. The thermal impedances of power devices can be extracted from the cooling curve obtained by applying a step power on each device, and can be further simplified into a series of Foster RC network by curve-fitting [28]. Fig. 19 shows the self and mutual thermal impedance of IGBT from the data-sheet and testing. It can be found that the self thermal impedances from the data-sheet and testing are different, and the amplitude of mutual thermal impedances is about one third of the self thermal impedance during the steady-state. Thus, it is necessary to conduct the thermal modeling and to take thermal coupling into account especially for the steady-state junction temperature estimation.

In order to validate the thermal model, a series of simulations and experiments are conducted to demonstrate the temperature response of the DUT. Fig. 21 shows the simulated and experimental steady-state temperatures of all the four devices under the operating condition as listed in Table III but with different currents ($I_0 = 7.13$ A, and $I_1 = 17.85$ A) and the frequency of 1 Hz. The shape and the amplitude of temperature variation obtained from simulation resembles the experiments.

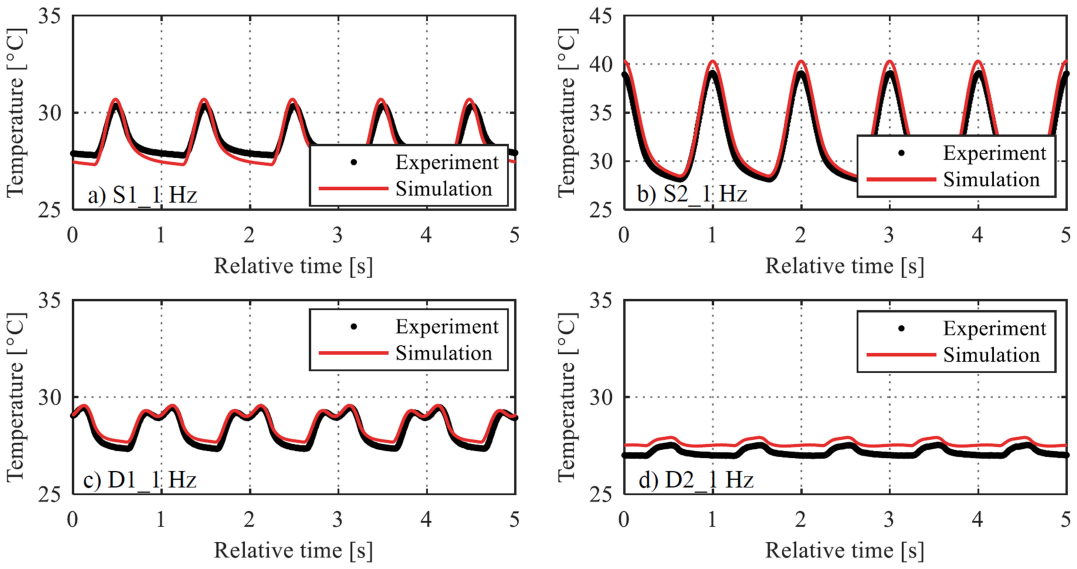

Fig. 21. Measured and simulated waveforms of the steady state junction temperature of the four devices with the frequency being 1 Hz. (a) S_1, (b) S_2, (c) D_1, and (d) D_2.

A difference up to $0.6\,^{\circ}\mathrm{C}$ can be observed for the average temperatures of the four devices. It can also be seen that device S_2 is the most stressed component under this operating condition, and it is due to the existence of an inherent DC bias in the arm current when the active power is transferred through the MMCs. The uneven thermal distribution will pose large thermal stress on specific component and finally accelerate the degradation of the SM as a whole. Thus, thermal balancing among devices is deserved to be studied to fulfill the lifetime potential of one SM.

Fig. 20 shows the junction temperature of the most stressed device S_2 with different temperature frequencies ranging from 50 Hz to 0.1 Hz. It can be seen that the simulated temperature swings agree well with the experiments with the largest error of $0.88\,^{\circ}\mathrm{C}$ when the frequency is 1 Hz. As for the average temperature, the temperature error goes down from $1.5\,^{\circ}\mathrm{C}$ to $0.2\,^{\circ}\mathrm{C}$ with the decrease of frequency from 50 Hz to 0.1 Hz.

VI. Conclusion

A mission profile emulator is proposed to assess the thermal behavior and the reliability of the power modules in the MMC. The use of the voltage stabilizer decouples the power supply voltage with the DUT, and the switching profile with the current profile. The voltage requirement for the DC power supply is greatly reduced, and any practical switching profile can be tested. Moreover, two capacitor voltage control strategies applicable to mission profiles with different switching frequencies are proposed. Also, some practical considerations for the setup implementation are discussed in order to guide the controller and hardware design. The feasibility for AC power cycling testing and thermal model validation has also been investigated. A series of simulation and experimental results have shown the effectiveness of the proposed mission profile emulator.

Appendix

The arm current considering the current ripple is

$$i_{\mathrm{arm}} = I_0 + I_1 \sin(\omega t + \varphi_1) + I_{\mathrm{r\_max}} \sin(\omega_{\mathrm{c}} t + \varphi_{\mathrm{r}}), \quad (17)$$

where the triangle current ripple is overlapped by a sinusoidal waveform, and ω_{c} and φ_{r} are the angular frequency and the initial phase angle of the carrier in the current source.

Since the carrier frequency is far higher than the fundamental frequency, the relationship below can be achieved

$$\int_0^{t_2} \sin(\omega_{\mathrm{c}} t + \varphi_{\mathrm{r}}) dt \approx \int_0^{t_2} \sin(2\omega_{\mathrm{c}} t + \varphi_{\mathrm{r}}) dt \approx 0 \quad (18)$$

where t_2 is the time interval of integral, namely $(T/2 + 2t_1)$ or $(T/2 - 2t_1)$.

$\omega_{\mathrm{c}} \pm \omega$ can be approximated by ω_{c} since it is larger than ω. $P(I_0, I_1)$ and $P(I_{\mathrm{r\_max}})$ can be estimated by (19) and (20)

$$P(I_0, I_1) = \frac{1}{T}\left(t_1\left(C_1 + \frac{C_3}{2}\right) + \frac{\sqrt{4 - m^2\cos^2\varphi_1}}{2\omega}\left(4C_2 - C_3 m\cos\varphi_1\right)\right) \quad (19)$$

$$\begin{aligned} P(I_{\mathrm{r\_max}}) &= \frac{1}{T}\left(\frac{2C_4}{\omega + \omega_{\mathrm{c}}}\sin\varphi_2 \cos\left(t_1(\omega + \omega_{\mathrm{c}})\right) + \frac{2C_4}{\omega - \omega_{\mathrm{c}}}\sin\varphi_2\cos\left(t_1(\omega - \omega_{\mathrm{c}})\right) + C_5 t_1 \right) \\ &\approx \frac{1}{T}\left(-\frac{2C_4}{\omega_{\mathrm{c}}} m\cos(\omega t_1)\sin\varphi_2\sin(\omega t_1) + C_5 t_1 \right) \\ &\le \frac{1}{T}\left(\frac{C_4}{\omega_{\mathrm{c}}} m\sqrt{4 - m^2\cos^2\varphi_1} + C_5 t_1 \right) \\ &= P_{\max}(I_{\mathrm{r\_max}}) \end{aligned} \quad (20)$$

where $C_1 = I_0 V_{\mathrm{on}} + I_0^2 R_{\mathrm{on}}$, $C_2 = 2I_0 I_1 R_{\mathrm{on}} + I_1 V_{\mathrm{on}}$, $C_3 = I_1^2 R_{\mathrm{on}}$, $C_4 = 2I_1 I_2 R_{\mathrm{on}}$ and $C_5 = I_2^2 R_{\mathrm{on}}$.

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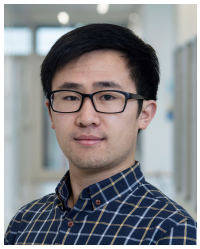

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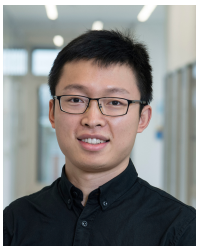

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